Octal LNA/VGA/AAF/ADC and CW I&Q Demodulator

Preliminary Technical Data

AD9276

FEATURES

8 channels of LNA, VGA, AAF, ADC and I&Q Demodulator
Low noise preamplifier (LNA)
- **Input-referred noise = 0.75 nV/√Hz (gain = 21.3 dB) @ 5 MHz typical**
- **SPI-programmable gain = 15.6 dB/17.9 dB/21.3 dB**
- **Single-ended input; V_{IN} maximum = 733 mV p-p/ 550 mV p-p/367 mV p-p**
- **Dual-mode active input impedance matching**
- **Bandwidth (BW) > 100 MHz**
- **Full-scale (FS) output = 4.4 V p-p differential**

Variable gain amplifier (VGA)
- **Attenuator range = −42 dB to 0 dB**
- **Postamp gain = 21 dB/24 dB/27 dB/30 dB**
- **Linear-in-dB gain control**

Antialiasing filter (AAF)
- **Programmable 2nd-order LPF from 8 MHz to 18 MHz**
- **Programmable HPF**

Analog-to-digital converter (ADC)
- **12 bits at 10 MSPS to 80 MSPS**
- **SNR = 70 dB**
- **SFDR = 75 dB**
- **Serial LVDS (ANSI-644, IEEE 1596.3 reduced range link)**
- **Data and frame clock outputs**

CW Mode I & Q demodulator
- **Invididualprogrammable phase rotation**
- **Output dynamic range per channel > 160dBc/√Hz**

Low power, 195 mW per channel at 12 bits/40 MSPS (TGC)
90 mW per channel for CW Doppler
Flexible power-down modes
Overload recovery in <10 ns
Fast recovery from low power standby mode, <2 µs
100-lead TQFP-EP

APPLICATIONS

Medical imaging/ultrasound
Automotive radar

GENERAL DESCRIPTION

The AD9276 is designed for low cost, low power, small size, and ease of use. It contains eight channels of a variable gain amplifier (VGA) with a low noise preamplifier (LNA); an antialiasing filter (AAF); a 12-bit, 10 MSPS to 80 MSPS analog-to-digital converter (ADC); and an I&Q demodulator with programmable phase rotation

Each channel features a variable gain range of 42 dB, a fully differential signal path, an active input preamplifier termination, a maximum gain of up to 52 dB, and an ADC with a conversion rate of up to 80 MSPS. The channel is optimized for dynamic performance and low power in applications where a small package size is critical.

The LNA has a single-ended-to-differential gain that is selectable through the SPI. The LNA input noise is typically 0.75 nV/√Hz at a gain of 21.3 dB, and the combined input-referred noise of the entire channel is 0.85 nV/√Hz at maximum gain. Assuming a 15 MHz noise bandwidth (NBW) and a 21.3 dB LNA gain, the input SNR is roughly 92 dB. In CW Doppler mode, each LNA output drives an I & Q demodulator. Each demodulator has independently programmable phase rotation through the SPI with 16 phase settings.

FUNCTIONAL BLOCK DIAGRAM

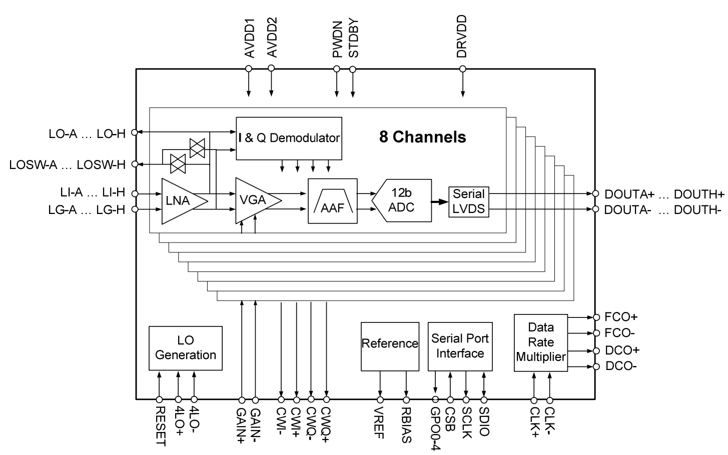

Figure 1

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

The AD9276 requires a LVPECL-/CMOS-/LVDS-compatible sample rate clock for full performance operation. No external reference or driver components are required for many applications.

The ADC automatically multiplies the sample rate clock for the appropriate LVDS serial data rate. A data clock (DCO±) for capturing data on the output and a frame clock (FCO±) trigger for signaling a new output byte are provided.

Powering down individual channels is supported to increase battery life for portable applications. There is also a standby mode option that allows quick power-up for power cycling. In CW Doppler operation, the VGA, AAF, and ADC are powered down. The power of the TGC path scales with selectable ADC speed power modes.

The ADC contains several features designed to maximize flexibility and minimize system cost, such as a programmable clock, data alignment, and programmable digital test pattern generation. The digital test patterns include built-in fixed patterns, built-in pseudorandom patterns, and custom user-defined test patterns entered via the serial port interface.

Fabricated in an advanced CMOS process, the AD9276 is available in a 16 mm × 16 mm, RoHS compliant, 100-lead TQFP. It is specified over the industrial temperature range of −40°C to +85°C.

PRODUCT HIGHLIGHTS

1. Small Footprint. Eight channels are contained in a small, space-saving package. Full TGC path, ADC, and I & Q demodulator contained within a 100-lead, 16 mm × 16 mm TQFP.
2. In TGC mode, low power of 190 mW per channel at 40 MSPS.
3. In CW mode, ultra-low power of 90mW per channel.
4. Integrated high dynamic range I & Q demodulator with phase rotation.
5. Ease of Use. A data clock output (DCO±) operates up to 480 MHz and supports double data rate (DDR) operation.
6. User Flexibility. Serial port interface (SPI) control offers a wide range of flexible features to meet specific system requirements.
7. Integrated Second-Order Antialiasing Filter. This filter is placed before the ADC and is programmable from 8 MHz to 18 MHz.

OUTLINE DIMENSIONS

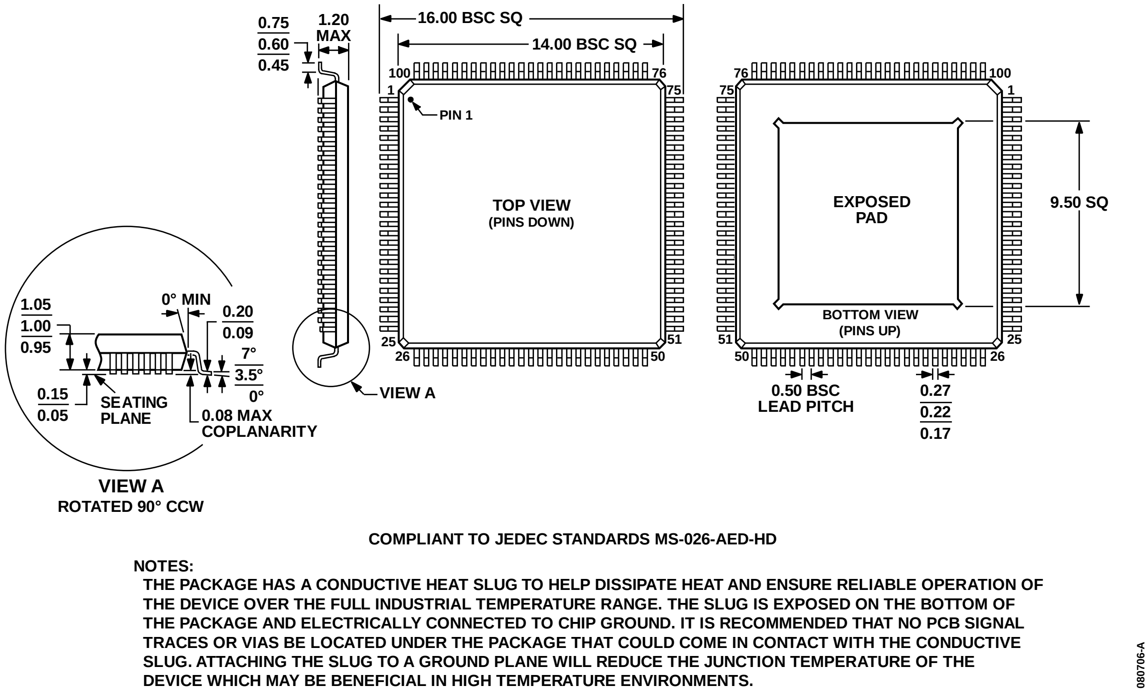

Figure 72. 100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]
(SV-100-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9276BSVZ	–40°C to +85°C	100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	SV-100-3
AD9276BSVZRL	–40°C to +85°C	100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP] Tape and Reel	SV-100-3
AD9276-65EBZ		Evaluation Board	
AD9276-80KITZ		Evaluation Board and High Speed FPGA based Data Capture Board	

NOTES

PR08180-0-4/09(PrB)